Claims

[c1] An arrangement for reducing non-linearity within an active resistor network, comprising:

a first active device adapted to provide resistance of a desired resistor, said first active device having a non-linear response; and

a second active device coupled to said first active device, said second active device having a non-linear response adapted to compensate substantially for said non-linear response of said first active device.

[c2] The arrangement of claim 1 wherein said first active device is coupled to receive control signals for regulating said resistance of said arrangement.

[c3] The arrangement of claim 2 wherein said second active device is coupled to receive control signals for regulating said resistance of said arrangement.

[c4] The arrangement of claim 3 wherein one of said first and second active devices is a p-type device and the other of said first and second active devices is an n-type device.

[c5] The arrangement of claim 4 wherein said first and said second active devices are CMOS devices.

[c6] The arrangement of claim 5 wherein said first and said second

active devices are provided with minimum dimensions for optimal high frequency performance.

[c7] The arrangement of claim 6 wherein said first and said second active devices are tuned using an optimisation algorithm.

[c8] The arrangement of claim 6 wherein said first and said second active devices are tuned using a manual tuning technique.

[c9] An active resistor network comprising an arrangement, said arrangement comprising a first active device adapted to provide resistance of a desired resistor, said first active device having a non-linear response; and a second active device coupled to said first active device, said second active device having a non-linear response adapted to compensate substantially for said non-linear response of said first active device.

[c10] The network of claim 9 wherein said first active device is coupled to receive control signals for regulating said resistance of said arrangement.

[c11] The network of claim 10 wherein said second active device is coupled to receive control signals for regulating said resistance of said arrangement.

[c12] The network of claim 11 wherein one of said first and said second active devices is a p-type device and the other of said

first and said second active devices is an n-type device.

[c13] The network of claim 12 wherein said first and said second active devices are CMOS devices.

[c14] The network of claim 13 wherein said first and said second active devices are provided with minimum dimensions for optimal high frequency performance.

[c15] The network of claim 14 wherein said first and said second active devices are tuned using an optimisation algorithm.

[c16] The network of claim 14 wherein said first and said second active devices are tuned using a manual tuning technique.

[c17] A method for reducing non-linearity within an active resistor network, comprising:
providing a first active device adapted to provide resistance of a desired resistor, the first active device having a non-linear response; and
providing a second active device coupled to the first active device, the second active device having a non-linear response adapted to compensate substantially for the non-linear response of the first active device.

[c18] The method of claim 17 wherein said first active device is coupled to receive control signals for regulating said resistance of said arrangement.

[c19] The method of claim 18 wherein said second active device is coupled to receive control signals for regulating said resistance of said arrangement.

[c20] The method of claim 19 wherein one of said first and said second active devices is a p-type device and the other of said first and said second active devices is an n-type device.

[c21] The method of claim 20 wherein said first and said second active devices are CMOS devices.

[c22] The method of claim 21 wherein said first and said second active devices are provided with minimum dimensions for optimal high frequency performance.

[c23] The method of claim 22 wherein said first and said second active devices are tuned using an optimisation algorithm.

[c24] The method of claim 22 wherein said first and said second active devices are tuned using a manual tuning technique.